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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/657,415 | 09/08/2003 | Elissa E. Carapella | 42P6139CD | 9024 |

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| EXAMINER | |
|---|---|
| NGUYEN, DONGHAI D | |
| **ART UNIT** | **PAPER NUMBER** |
| 3729 | |

DATE MAILED: 08/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/657,415 | CARAPELLA ET AL. | |
| | Examiner | Art Unit | |
| | Donghai D. Nguyen | 3729 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *17,18,24-32,36,37,41-45,47 and 48* is/are pending in the application.

4a) Of the above claim(s) *24-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17,18,31,32,36,37,41-45,47 and 48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

1. The amendment filed on May 15, 2006 has been considered and made of record.

### *Claim Objections*

2. Claims 42 and 43 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The limitations of claims 42 and 43 already find in the independent claim 17 (newly added subject matter).

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4. Claims 31, 32, 36, 37, 47 and 49 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

"second conductive strip of the pair of conductive strips coupled to a second bonding pads of the plurality of bonding pads" (claim 31, line 12-14) is not clear because it is not known if a second bonding pad is apart of the plurality of bonding pads as previously recited in line 7. It is suggested that "at least one of" in claim 31, line 7 should be deleted since there are more than one bonding pads being coupled to.

Whether: "the plurality of bonding pads" in claim 36, line 8 as same as "the first plurality of bonding pads" as previously recited in lines 4-5. Whether "a first and second bonding pads" (claim 36, lines 14-15) are both directed to "the first plurality of bonding pads" are apart of the plurality of the plurality of bonding pads or of "the first plurality of bonding pads". Please be consistent. It is suggested that "a first plurality of bonding pads" (lines 4-5) should be changed to: --a plurality of bonding pads--.

### *Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 17, 18, 31, 32, 41-45, 47 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5,825,084 to Lau et al in view of Applicant Admitted Prior Art (AAPA).

Regarding claim 17, Lau et al disclose a method of forming an integrated circuit package, comprising: providing a package housing having a first bonding pads (110' in Fig. 2A or 210 in Fig 4B) located on a first bond shelf (100, 200 etc.), the bond shelf including top surface and a fist edge (See Figs. 2A and 4B); forming a fist conductive strip (215 one surface of the central portion 105, see Fig 4B) along the first edge of the first bond shelf, the conductive strip wrapping around and over the first edge of the first bond shelf to electrically couple a first bonding pad (top bonding pad 210 in fig. 4B) of the first plurality of bonding pads (210) on the first the bond

shelf to a first power bus (140) under the first bond shelf (see Fig. 2A); and forming a second conductive strip (215 to the left or right of the central portion 205) along the first edge of the first bond shelf the second conductive strip wrapping around and over the first edge of the first bond shelf to electrically couple a second bonding pad (the left or right bonding pad shown in Fig. 4B) of the first plurality of bonding pads (210) on the first bond shelf to a second power bus (different power bus 140 see Fig. 2C) under the first bond shelf, the second power bus located with the first power bus in a same horizontal plane (bottom surface of the bonding shelf 200 or 500, see Figs 2 and 6) of the integrated circuit package. Lau et al do not disclose the second bus having a second voltage level less than the first voltage level of the first bus. However, AAPA teaches that the different voltage levels are required in some integrated circuit such as 3.3 volts and 2.0 volts (Spec. page 2, lines 15-17). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the power buses of Lau et al carry different voltage levels as taught by AAPA for supplying power to the integrated circuit that requires different voltage level.

Regarding claim 18, Lau et al disclose the conductive strip is formed by plating (Col. 5, lines 39-41).

Regarding claims 31 and 47, Lau et al disclose a method of forming an integrated circuit package, comprising: providing a package housing having a first bond shelf (100, 200 etc.) with a top surface and an inside surface (See Figs. 2A, 4B); forming a conductive material (215 see Fig. 4B) along the inside surface of the first bond shelf, a first portion of the conductive material wrapping around from the inside surface onto the top surface of the first bond shelf (Col. 4, lines

38-40) to form a plurality of bonding pads (110' or 210) on the top surface of the bond shelf (See Figs. 2A and 4C); and, removing a second portion (130 see Fig. 2A and Col. 5, lines 60-63) of the conductive material along the inside surface of the bond shelf to form a pair of separate conductive strips along the inside surface of the bond shelf (see Figs. 2A, 3D, 4D) with a first conductive strip (middle strip 215' in Fig. 4D) of the pair of conductive strips coupled to a first bonding pad of the plurality of bonding pads coupled to a first power bus (140) and a second conductive strip (right strip 215' in Fig. 4D) of the pair of conductive strips coupled to a second bonding pad of the plurality of bonding pads coupled to a second power bus (another 140 see Fig. 2C), the second power bus located with the first power bus in a same horizontal plane (bottom surface of the bonding shelf 200 or 500, see Figs 2 and 6) of the integrated circuit package. Lau et al do not disclose the second bus having a second voltage level less than the first voltage level of the first bus. However, AAPA teaches that the different voltage levels are required in some integrated circuit such as 3.3 volts and 2.0 volts (Spec. page 2, lines 15-17). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the power buses of Lau et al carry different voltage levels as taught by AAPA for supplying power to the integrated circuit that requires different voltage level.

Regarding claim 32, Lau et al disclose the conductive strip is formed by plating (Col. 5, lines 39-41).

Regarding claims 36 and 49, Lau et al disclose a method of forming an integrated circuit package (see Fig. 1B), comprising: providing a package housing having a rectangular bond shelf (100, 200 etc.) with a rectangular top surface and an inside surface perpendicular with the top surface (See Figs. 2A, 4B), the bond shelf having a first plurality of bonding pads (110'/210)

located on the top surface; forming a conductive material (Col. 5, lines 32-33) along the side surface of the bond shelf, a first portion of the conductive material wrapping around from the inside surface onto the top surface of the bond shelf (Col. 4, lines 38-40) to couple to at least one of the first plurality of bonding pads on the top surface of the bond shelf (See Fig. 4C); and, removing a second portion (130) of the conductive material along the inside surface of the bond shelf to form a pair of separate conductive strips along the inside surface of the bond shelf (see Figs. 2A, 3D, 4D) with a first conductive strip (middle strip 215' in Fig. 4D) of the pair of conductive strips coupled to a first bonding pad of the plurality of bonding pads coupled to a first power bus (140) and a second conductive strip (right strip 215` in Fig. 4D) of the pair of conductive strips coupled to a second bonding pad of the plurality of bonding pads coupled to a second power bus (another 140 see Fig. 2C), the second power bus located with the first power bus in a same horizontal plane (bottom surface of the bonding shelf 200 or 500, see Figs 2 and 6) of the integrated circuit package. Lau et al do not disclose the second bus having a second voltage level less than the first voltage level of the first bus. However, AAPA teaches that the different voltage levels are required in some integrated circuit such as 3.3 volts and 2.0 volts (Spec. page 2, lines 15-17). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the power buses of Lau et al carry different voltage levels as taught by AAPA for supplying power to the integrated circuit that requires different voltage level.

Regarding claim 37, Lau et al disclose the conductive strip is formed by plating (Col. 5, lines 39-41).

Regarding claim 41, Lau et al disclose forming the conductive strips by removing a portion of conductive strip (Col. 5, lines 60-63).

Regarding claim 42, Lau et al disclose the power buses are located on the same plane (see Fig. 2C).

The limitations claims 43-45, 47 and 29 also met as set forth above.

### *Response to Arguments*

7. Applicant's arguments with respect to claims 17, 18, 31, 32, 41-45, 47 and 49 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghai D. Nguyen whose telephone number is (571)-272-4566. The examiner can normally be reached on Monday-Friday (9:00-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter D. Vo can be reached on (571)-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DN

July 25, 2006

MINH TRINH
PRIMARY EXAMINER